

### In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1           1. (Original) A method of operating an integrated circuit  
2 including read accessible memory comprising the steps of:  
3           testing memory read operations beginning at a maximum speed at  
4 successively slower speeds until all memory reads pass;  
5           determining memory read program bits for a highest memory  
6 speed passing the memory read tests; and  
7           programming write once bits according to determined memory  
8 read program bits.

1           2. (Original) The method of claim 1 further comprising the  
2 steps of:  
3           preliminary soft programming determined bits; and  
4           testing non-memory portions of the integrated circuit using  
5 soft programmed determined memory read program bits.

1           3. (Original) The method of claim 1 wherein:  
2 said step of programming write once bits includes  
3           applying program voltages to the bits,  
4           testing the write once bits to determine achieved  
5 programming, and  
6           repeating applying program voltages and testing the write  
7 once bits until the testing confirms correct write once bit  
8 programming.

1           4. (Original) The method of claim 1 wherein programming of  
2 eFuse bits includes:  
3           merging of programming of write once bits for memory read  
4 speed with programming write once bits not related to memory speed.

1        5. (Original) The method of claim 4 wherein:  
2        the write once bits not related to memory speed include a  
3        specific die-identification bit code.

1        6. (Original) The method of claim 4 wherein:  
2        the write once bits not related to memory read speed include  
3        write once bits for memory redundancy programming.

1        7. (Original) The method of claim 4 wherein:  
2        the write once bits not related to memory read speed include  
3        write once bits for control of programmable logic functions.

1        8. (Original) The method of claim 1, wherein the read  
2        accessible memory is write accessible, further comprising:  
3        testing memory write operations beginning at a maximum speed  
4        at successively slower speeds until all memory reads pass;  
5        determining memory write program bits for a highest memory  
6        speed passing the memory write tests; and  
7        said step of programming write once bits according to  
8        determined memory read program bits further includes programming  
9        write once bits according determined memory write program bits.

1        9. (Original) A method of operating an integrated circuit  
2        including write accessible memory comprising the steps of:  
3        testing memory write operations beginning at a maximum speed  
4        at successively slower speeds until all memory writes pass;  
5        determining memory write program bits for a highest memory  
6        speed passing the memory write tests; and  
7        programming write once bits according to determined memory  
8        write program bits.

1        10. (Original) The method of claim 9 further comprising the  
2 steps of:  
3        preliminary soft programming determined write once bits; and  
4        testing non-memory portions of the integrated circuit using  
5 soft programmed determined memory write program bits.

1        11. (Original) The method of claim 9 wherein:  
2 said step of programming write once bits includes  
3        applying program voltages to the write once bits,  
4        testing the write once bits to determine achieved  
5 programming, and  
6        repeating applying program voltages and testing the write  
7 once bits until the testing confirms correct write once bit  
8 programming.

1        12. (Original) The method of claim 9 wherein:  
2 programming of write once bits includes merging of programming  
3 of write once bits for memory write speed with programming write  
4 once bits not related to memory speed.

1        13. (Original) The method of claim 12 wherein:  
2 the write once bits not related to memory write speed include  
3 a specific die-identification bit code.

1        14. (Original) The method of claim 12 wherein:  
2 the write once bits not related to memory write speed include  
3 write once bits for memory redundancy programming.

1        15. (Original) The method of claim 12 wherein:  
2 the write once bits not related to memory write speed include  
3 write once bits for control of programmable logic functions.

16 to 18. (Canceled)

1 19. (New) The method of claim 1 further comprising the steps  
2 of:  
3 operating memory read operations of the read accessible memory  
4 at a speed corresponding to the programmed write once memory read  
5 program bits.

1 20. (New) The method of claim 8 further comprising the steps  
2 of:  
3 operating memory write operations of the read accessible  
4 memory at a speed corresponding to the programmed write once memory  
5 write program bits.

1 21. (New) The method of claim 9 further comprising the steps  
2 of:  
3 operating memory write operations of the write accessible  
4 memory at a speed corresponding to the programmed write once memory  
5 write program bits.